CLAIMS

What is claimed is:

1. A multi-chips stacked package, comprising:

a substrate having an upper surface, a lower surface and an opening passing through the upper surface and the lower surface;

an upper chip having a first active surface and a first back surface, wherein the upper chip is flipped over and attached to the upper surface of the substrate via a plurality of first electrically conductive bumps;

a lower chip accommodated in the opening and electrically connected to the first active surface of the upper chip through a plurality of second electrically conductive bumps; and

a reinforced bump interposed between the substrate and the upper chip.

2. The multi-chips stacked package of claim 1, further comprising an underfill filled into the opening.

3. The multi-chips stacked package of claim 2, wherein the underfill covers the first electrically conductive bumps and the second electrically conductive bumps.

4. The multi-chips stacked package of claim 1, wherein the upper chip covers the opening.

5. The multi-chips stacked package of claim 1, wherein the reinforced bump is located at a corner of the active surface of the upper chip.

6. The multi-chips stacked package of claim 1, wherein the reinforced bump is located at a periphery of the first active surface of the upper chip.

7. The multi-chips stacked package of claim 1, wherein the reinforced bump is

close to the perimeter of the opening.

8. The multi-chips stacked package of claim 1, wherein the reinforced bump is a ring-like bump.

9. The multi-chips stacked package of claim 1, wherein the reinforced bump is a bar-like bump.

10. The multi-chips stacked package of claim 2, wherein the underfill covers the reinforced bump.

11. The multi-chips stacked package of claim 1, wherein the reinforced bump is a solder bump.

12. The multi-chips stacked package of claim 11, wherein the material of the reinforced bump comprises lead and tin.

13. The multi-chips stacked package of claim 12, wherein the ratio of the lead and the tin is 95:5.

14. The multi-chips stacked package of claim 2, wherein the lower chip has a second back surface exposing out of the underfill.

15. The multi-chips stacked package of claim 1, further comprising a plurality of solder balls formed on the lower surface of the substrate.

16. The multi-chips stacked package of claim 1, wherein the reinforced bump is made of epoxy.

17. The multi-chips stacked package of claim 1, wherein the upper chip is larger than the lower chip in size.

18. The multi-chips stacked package of claim 2, wherein the underfill covers a portion of the first active surface of the upper chip.

19. The multi-chips stacked package of claim 2, wherein the underfill entirely covers the first active surface of the upper chip.

20. The multi-chips stacked package of claim 2, wherein the underfill covers a portion of the upper surface of the substrate.

21. A multi-chips stacked package, comprising:

a substrate having an upper surface and a lower surface;

an upper chip having a first active surface and a first back surface, wherein the upper chip is flipped over and attached to the upper surface of the substrate via a plurality of first electrically conductive bumps;

a lower chip interposed between the upper surface of the substrate and the first active surface of the upper chip and electrically connected to the first active surface of the upper chip through a plurality of second electrically conductive bumps; and

a reinforced bump interposed between the upper surface of the substrate and the first active surface of the upper chip.

22. The multi-chips stacked package of claim 21, wherein each of the first electrically conductive bumps is larger than each of the second electrically conductive bumps in height.

23. The multi-chips stacked package of claim 21, wherein each of the first electrically conductive bumps is substantially equal to the reinforced bump in height.